

a first element isolation region provided in the semiconductor substrate, the first element isolation region isolating the first element region;

a second element isolation region provided in the semiconductor substrate, the second element isolation region isolating the second element region;

a first transistor having source and drain diffusion layers each provided in the first element region;

a second transistor having source and drain diffusion layers each provided in the second element region; and

an insulating film covering the first and second transistors, (the insulating film being harder for an oxidizing agent to pass therethrough, compared with a silicon oxide film, and the insulating film being oxidized.)

27. (New) The device according to claim 26, wherein surfaces of gate electrodes of the first and second transistors are oxidized.

28. (New) The device according to claim 26, wherein the insulating film has a thickness of at most 50 nm.

29. (New) The device according to claim 26, wherein the insulating film includes a silicon nitride film.

30. (New) The device according to claim 29, wherein a surface of the silicon nitride film is oxidized.

31. (New) The device according to claim 30, wherein a thickness of an oxidized region of the silicon nitride film is at least 1 nm and at most 10 nm.

32. (New) The device according to claim 29, wherein the silicon nitride film contains hydrogen, and a concentration of the hydrogen is at most  $3 \times 10^{21}$  atom/cm<sup>3</sup>.

~~33.~~ (New) The device according to claim 29, wherein the silicon nitride film contains hydrogen, and a concentration of the hydrogen gradually becomes higher from the surface of the silicon nitride film.

~~34.~~ (New) The device according to claim 26, wherein a gate electrode of each of the first and second transistors contains a metal or a metal silicide.

~~35.~~ (New) The device according to claim 34, wherein the metal contains tungsten.

~~36.~~ (New) The device according to claim 26, wherein a gate electrode of each of the first and second transistors is a stacked gate structure including a floating gate and a control gate, and the control gate contains a metal or a metal silicide.

~~37.~~ (New) The device according to claim 36, wherein the metal contains tungsten.

~~38.~~ (New) The device according to claim 26, further comprising:

a third transistor having source and drain diffusion layers each provided in the second element region,

wherein the second transistor includes an erasable and programmable memory cell transistor and the third transistor includes a selection gate transistor.

~~39.~~ (New) The device according to claim 38, wherein a gate electrode of the erasable and programmable memory cell transistor and a gate electrode of the selection gate transistor are stacked gate structures including a floating gate and a control gate, and the control gate contains a metal or a metal silicide.

~~40.~~ (New) The device according to claim 39, wherein the metal contains tungsten.

~~41.~~ (New) The device according to claim 40, wherein the floating gate of the selection gate transistor is electrically connected to the control gate of the selection gate transistor.

~~42.~~ (New) The device according to claim 26, wherein the second transistor includes an erasable and programmable memory cell transistor.

43. (New) The device according to claim 42, wherein a gate electrode of the erasable and programmable memory cell transistor is a stacked gate structure including a floating gate and a control gate, and the control gate contains a metal or a metal silicide.

44. (New) The device according to claim 43, wherein the metal contains tungsten.

45. (New) A nonvolatile semiconductor memory device, comprising:  
a semiconductor substrate having a peripheral circuit region and a memory cell region;  
a first element region provided in the peripheral circuit region;  
a second element region provided in the memory cell region;  
a first element isolation region provided in the semiconductor substrate, the first element isolation region isolating the first element region;  
a second element isolation region provided in the semiconductor substrate, the second element isolation region isolating the second element region;  
a first transistor having source and drain diffusion layers each provided in the first element region;  
a second transistor having source and drain diffusion layers each provided in the second element region; and  
an insulating film covering the first and second transistors and the first and second element isolation regions, the insulating film being harder for an oxidizing agent to pass therethrough, compared with a silicon oxide film, and the insulating film being oxidized.

46. (New) The device according to claim 45, further comprising:  
an inter-level insulating film provided on the insulating film, the inter-level insulating film containing another insulator different from the insulating film;

a contact hole provided in the inter-level insulating film and the insulating film, and reaching at least one of the source and drain diffusion layers of the second transistor; and

a contact provided in the contact hole, the contact electrically connected to the at least one of the source and drain diffusion layers of the second transistor.

47. (New) The device according to claim 46, wherein the insulating film is an etching stopper of the contact hole for the second element isolation region.

48. (New) The device according to claim 46, wherein the contact hole overlaps the second element isolation region.

49. (New) The device according to claim 48, wherein a diameter of the contact hole is wider than a width of the second element region.

50. (New) The device according to claim 46, further comprising:

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another insulating film provided under the insulating film and over the first and second transistors and over the first and second element isolation regions, the another insulating film containing another insulator different from the insulating film.

*A* 51. (New) The device according to claim 45, wherein surfaces of gate electrodes of the first and second transistors are oxidized.

52. (New) The device according to claim 45, wherein the insulating film has a thickness of at most 50 nm.

53. (New) The device according to claim 45, wherein the insulating film includes a silicon nitride film.

54. (New) The device according to claim 53, wherein a surface of the silicon nitride film is oxidized.

55. (New) The device according to claim 54, wherein a thickness of an oxidized region of the silicon nitride film is at least 1 nm and at most 10 nm.

~~56.~~ (New) The device according to claim 53, wherein the silicon nitride film contains hydrogen, and a concentration of the hydrogen is at most  $3 \times 10^{21}$  atom/cm<sup>3</sup>.

~~57.~~ (New) The device according to claim 53, wherein the silicon nitride film contains hydrogen, and a concentration of the hydrogen gradually becomes higher from the surface of the silicon nitride film.

~~58.~~ (New) The device according to claim 45, wherein a gate electrode of each of the first and second transistors contains a metal or a metal silicide.

~~59.~~ (New) The device according to claim 58, wherein the metal contains tungsten.

~~60.~~ (New) The device according to claim 45, wherein a gate electrode of each of the first and second transistors is a stacked gate structure including a floating gate and a control gate, and the control gate contains a metal or a metal silicide.

~~61.~~ (New) The device according to claim 60, wherein the metal contains tungsten.

~~62.~~ (New) The device according to claim 45, further comprising:

a third transistor having source and drain diffusion layers each provided in the second element region,

wherein the second transistor includes an erasable and programmable memory cell transistor and the third transistor includes a selection gate transistor.

~~63.~~ (New) The device according to claim 62, wherein a gate electrode of the erasable and programmable memory cell transistor and a gate electrode of the selection gate transistor are stacked gate structures including a floating gate and a control gate, and the control gate contains a metal or a metal silicide.

~~64.~~ (New) The device according to claim 63, wherein the metal contains tungsten.